Serial Peripheral Interface (SPI)

Serial Peripheral Interface is a 4-wire communication protocol between two or more devices in which one serves as the controller or master while the other(s) serves as the slave. It is a two-way communication protocol enabling exchange of data between the devices. The master initiates communication while the slaves respond.

**Key Features:**

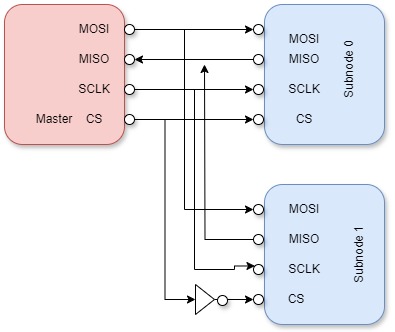
1. Full-duplex communication

2. Master-slave architecture

3. Synchronous data transfer

4. High-speed data transfer (up to 100 Mbps)

|  |  |  |
| --- | --- | --- |
|  | Advantages | Disadvantages |
| 1. | Simple and low-cost implementation | Limited distance (typically up to 10 meters) |
| 2. | High-speed data transfer | Requires separate clock and data lines |
| 3. | Flexible communication protocol | Not suitable for multi-master systems |



**Key Components:**

1. Master (initiates communication):

2. Slave (responds to master)

3. Clock (SCK): Clock signal generated by the master

4. Data Out (MOSI): port used for data transmission from master to slave

5. Data In (MISO): port used for data transmission from the slave sub node.

6. Chip Select (CS): Slave select signal (active low).

**SPI Modes:**

1. Mode 0: CPOL=0, CPHA=0 (Clock idle low, data captured on rising edge)

2. Mode 1: CPOL=0, CPHA=1 (Clock idle low, data captured on falling edge)

3. Mode 2: CPOL=1, CPHA=0 (Clock idle high, data captured on falling edge)

4. Mode 3: CPOL=1, CPHA=1 (Clock idle high, data captured on rising edge)

**Applications:**

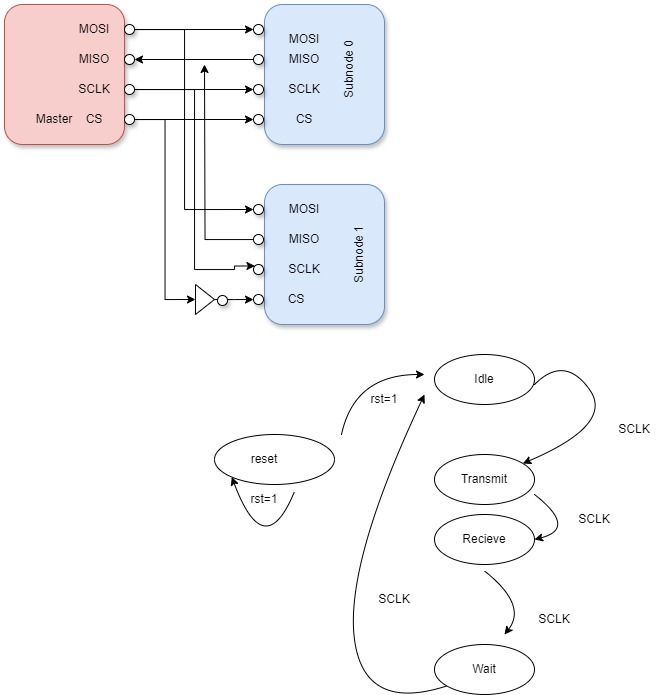
1. Sensor interfaces
2. Display interfaces
3. SD card reader interface
4. Embedded System and Microcontrollers

**Design Specification**

Data width: 8 Bits

SPI Controller States: IDLE, TRANSMIT, RECEIVE, WAIT. This is indicated by the status register. When the State is **IDLE**, this is the initial state, after a reset has cleared all register to **8’d0**, the master device is not communicating with the slave device. The master transmit register is then set with the data bits to transmit and SS pin is active to select the slave device. The master’s shift register then transfer the data to the slave. The state changes to TRANSMIT when the master is sending the data to the slave through the MOSI data pin. the

**Transition Diagram:**



MASTER